REMARKS

These remarks are in response to the fourth, final Office Action mailed on May 3, 2002. The Office Action maintained its previous rejection of claims 1-42. Although claims 1, 2, 12-14, 31, 32 and 35 are believed allowable for the reasons given in the previous response, they have been cancelled to facilitate the application process. Claims 15 and 33 have been rewritten in independent form by incorporating their underlying claims. All of the independent claims have been amended to further specify that the recited anti-reflective layer (ARL) is an anti-reflective layer for use in a photolithographic process. These claims are respectfully submitted to be allowable over the prior art. Although believed allowable in their previous form, they have been so amended to further clarify their distinctions over the prior art.

All of the pending claims recite the use of an anti-reflective layer (ARL) as part of a photolithographic process. As described in the present application between page 1, line 8, and page 2, line 6, is a layer used during the formation of integrated circuits and is placed formed over the structure before the formation of a photolithographic mask. The ARL absorbs the majority of radiation that penetrates the resist by being less reflective than the surface upon which it is placed would otherwise be.

The Office Action rejects independent claims 3, 15, 36, and 40 under 35 U.S.C. 102(a) as being anticipated by Kayanuma et al. (U.S. patent number 5,397,729). This is respectfully submitted to be in error. The Kayanuma reference has no teachings as to the use of antireflective layers for use in photolithographic process. The cited feature in the Office Action (layer 59 of Figure 4e) is a metal silicide layer. Such layers are used to improve the conductivity of underlying poly layers, here transistor gate 52, and are not used as an antireflective layers in photolithographic processes since they do not significantly reduce the reflectively of the underlying layer, instead often increasing the amount of reflectivity compared to an underlying layer not so coated, and do not form on oxides. Therefore, it is respectfully submitted that a rejection of claims 3, 15, 36, and 40 (and their dependent claims 8-10, 16-25, 37-39, and 41-42) under 35 U.S.C. 102(a) based on Kayanuma is not well founded.

The Office Action rejects independent claim 26 under 35 U.S.C. 102(a) as being anticipated by Takahashi et al. (U.S. patent number 5,618,749). This also is respectfully submitted to be in error. The Takahashi reference also has no teachings as to the

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

use of antireflective layers for use in photolithographic process. As with the Kayanuma reference, the cited feature in the Office Action (layer 6b of Figure 9) is a metal silicide layer and is used for the same purpose as in the Kayanuma reference. Therefore, it is respectfully submitted that a rejection of claim 26 and its dependent claims 27-30 under 35 U.S.C. 102(a) based on Takahashi is not well founded.

The Office Action rejects independent claims 4 and 33 under 35 U.S.C. 103(a) based on Kayanuma and the secondary reference of Wang et al. (U.S. patent number 5,545,585) that is cited to provide specific dimensions for the conformal insulating layer. This secondary reference also provides no teachings on the use of anti-reflective layers in photolithographic processes. Consequently, it is respectfully submitted that a rejection of claims 4 and 33 (and their dependent claims 5-7 and 34) under 35 U.S.C. 103(a) based on these references is also not well founded.

The various dependent claims are also believed allowable for reasons previously stated, but these will not be discussed in the present Amendment except for claims 40-42. Claims 40-42 are drawn to the feature that the flow is designed so that the capacitor module (steps 4-10a on page 9 of the application) is removable without altering the other portions of the flow shown on page 9 as steps 1-14. This is discussed, for example, on page 12, lines 11-16.

For any of these reasons, reconsideration of the Office Action's rejection of claims 3-11, 15-30, and 33-42 is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

EXPRESS MAIL LABEL NO:

Respectfully submitted,

Michael G. Cleveland
Reg. No. 46,030

Date

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
25th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

APPENDIX

Amended Claims

3.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

4.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0660

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

15.(Amended) A [The] method of [claim 14] forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

26.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

33.(Amended) A [The] method of [claim 32] forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

36.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the structure resultant from said forming a conformal layer;

forming a patterned mask over the structure resultant from said forming an ARL; and

etching said conductive layer using said patterned mask.

40.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

providing a process flow for etching said conductive layer, whereby the gates of one or more transistors are formed, said flow including a photolithographic process comprising:

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conductive layer; and

forming a patterned mask over said ARL, wherein said photolithographic process is optimized for forming said gates;

performing a capacitor formation process comprising:

forming one or more capacitor structures, each comprising a top electrode over a portion of said conductive layer and a dielectric layer between the top electrode and the conductive layer; and

forming a conformal insulating layer over said capacitor structures and at least a portion of said conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming said ARL, whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered; and

etching said conductive layer according to said process flow, whereby the lower electrodes of said capacitor structures and said gates are formed.

Pending Claims

(Claims 1 and 2 have been cancelled.)

3.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of th dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

4.(Twice Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

5. The method according to claim 4, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

6. The method according to claim 5, wherein said thermal process is a rapid thermal oxidation is performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range of from 850°C to 1050°C.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP
Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0040

7. The method according to claim 4, wherein said conformal insulating layer is formed by deposition.

8. The method of claim 3, wherein said ARL is an anti-reflective coating.

9. The method of claim 3, wherein said ARL is titanium nitride.

10. The method of claim 3, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

11. The method according to claim 10, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

(Claims 12-14 have been cancelled)

15.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an insulating layer over at least a portion of said top electrode and said exposed portion of the dielectric layer;

removing a portion of said insulating layer and a portion of said dielectric layer, thereby exposing at least a portion of said lower electrode and forming side wall spacers, wherein said side wall spacers are formed on the side walls of the top electrode and of the inter-electrode region of the dielectric; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent removing a portion of said insulating layer and a portion of said dielectric layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

16. The method according to claim 15, wherein said insulating layer is formed by deposition.

17.(Amended) The method according to claim 16, wherein prior to forming said insulating layer by deposition, an anneal is performed.

18. The method according to claim 15, wherein said insulating layer is grown.

19. The method according to claim 15, wherein said insulating layer is an oxide layer with a thickness in the range of from 500Å to 2000Å.

20. The method according to claim 15, wherein said side wall spacers have a width in the range of from 500Å to 2000Å.

21. The method according to claim 15, wherein said ARL is an anti-reflective coating.

22. The method according to claim 15, wherein said ARL is titanium nitride.

23. The method according to claim 15, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

24. The method according to claim 23, wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness in the range of from 300Å to 400Å.

25. The method according to claim 15, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

26.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer.on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of said top electrode and said exposed portion of the dielectric layer; and

subsequently removing a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors.

27. The method according to claim 26, wherein said ARL is an anti-reflective coating.

28. The method according to claim 26, wherein said ARL is titanium nitride.

29. The method according to claim 26, wherein said ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

30. The method according to claim 26, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

33.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
29th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å; and

forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said non-insulating layer is an anti-reflective layer (ARL) for use in a photolithographic process.

34. The method according to claim 33, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

(Claims 35 has been cancelled.)

36.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure;

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the structure resultant from said forming a conformal layer;

forming a patterned mask over the structure resultant from said forming an ARL; and

etching said conductive layer using said patterned mask.

37. The method according to claim 36, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

38. The method according to claim 37, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

39. The method according to claim 36, wherein said conductive layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

40.(Amended) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

providing a process flow for etching said conductive layer, whereby the gates of one or more transistors are formed, said flow including a photolithographic process comprising:

forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the conductive layer; and

forming a patterned mask over said ARL, wherein said photolithographic process is optimized for forming said gates;

performing a capacitor formation process comprising:

forming one or more capacitor structures, each comprising a top electrode over a portion of said conductive layer and a dielectric layer between the top electrode and the conductive layer; and

forming a conformal insulating layer over said capacitor structures and at least a portion of said conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming said ARL, whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered; and

etching said conductive layer according to said process flow, whereby the lower electrodes of said capacitor structures and said gates are formed.

41. The method according to claim 40, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

42. The method according to claim 41, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

Three Embarcadero Center
28th Floor
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646